SNx4HC08 Quadruple 2-Input Positive-AND Gates

1 Features

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive up to 10 LSTTL Loads
- Low Power Consumption: Maximum I_{CC} 20 µA
- Typical t_{pd} = 8 ns at 6 V
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 µA (Maximum)

2 Applications

- Servers
- LED Displays
- Network Switches
- I/O Expanders
- Base Station Processor Boards

3 Description

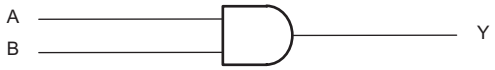
The SNx4HC08 devices contain four independent 2-input AND gates. They perform the Boolean function $Y = A \bullet B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HC08D	SOIC (14)	8.65 mm × 3.90 mm
SN74HC08DB	SSOP (14)	6.30 mm × 5.30 mm
SN74HC08N	PDIP (14)	19.34 mm × 6.35 mm
SN74HC08NS	SO (14)	10.30 mm × 5.30 mm
SN74HC08PW	TSSOP (14)	5.00 mm × 4.40 mm
SN54HC08	LCCC (20)	1.83 mm × 8.89 mm
	CDIP (14)	19.56 mm × 6.67 mm
	CFP (14)	9.21 mm × 5.97 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Diagram



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4 Revision History

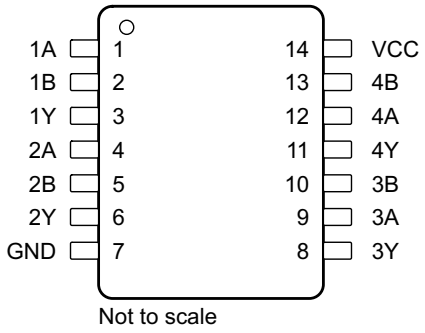
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (January 2007) to Revision G	Page
• Added *ESD Ratings* table,*Feature Description*section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations*section, *Layout*section, *Device and Documentation Support* section, and*Mechanical, Packaging, and Orderable Information* section	1
• Removed *Ordering Information* table, see POA at the end of the datasheet	1
• Added ESD warning	4
• Split *Electrical Characteristics* and *Switching Characteristics* tables into separate tables for the SN54HC08 and SN74HC08 parts	5

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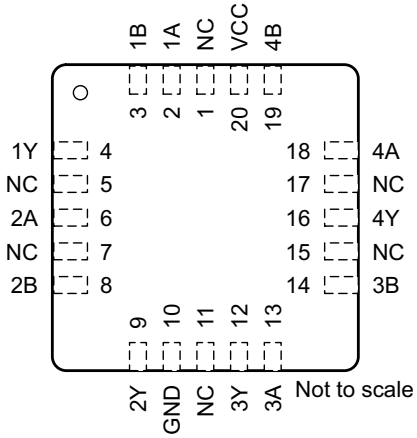
5 Pin Configuration and Functions

SN54HC08: J, W; SN74HC08: D, DB, N, NS, and PW Packages
14-Pin CDIP, CFP, SOIC, SSOP, PDIP, SO, and TSSOP
Top View



Not to scale

SN54HC08 FK Package
20-Pin LCCC
Top View



Not to scale

Pin Functions

PIN			I/O	DESCRIPTION
NAME	CDIP, CFP, SOIC, SSOP, PDIP, SO, and TSSOP	LCCC		
1A	1	2	I	Input 1
1B	2	3	I	Input 1
1Y	3	4	O	Output 1
2A	4	6	I	Input 2
2B	5	8	I	Input 2
2Y	6	9	O	Output 2
3A	9	13	I	Input 3
3B	10	14	I	Input 3
3Y	8	12	O	Output 3
4A	12	18	I	Input 4
4B	13	19	I	Input 4
4Y	11	16	O	Output 4
GND	7	10	—	Ground Pin
VCC	14	20	—	Power Pin
NC	—	1, 5, 7, 11, 15, 17	—	No internal connection

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage		–0.5	7	V
Input clamp current(2), I_{IK}	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
Output clamp current(2), I_{OK}	$V_O < 0$		±20	mA
Continuous output current, I_O	$V_O = 0$ to V_{CC}		±25	mA
Continuous current through VCC or GND, I_{CC}			±50	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
SN74HC08 in D, DB, N, NS, or PW				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Δt/Δv	Input transition rise and fall rate	V_{CC} = 2 V			1000	ns/V
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature	SN54HC08	–55		125	°C
		SN74HC08	–40		85	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

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6.4 Thermal Information

THERMAL METRIC(1)		SN74HC08					UNIT
		D (SOIC)	DB (SSOP)	N (CFP)	NS (SO)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.5	106.8	56.5	89.9	121.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.4	58.8	43.7	47.7	49.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.7	54.2	36.3	48.7	62.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.4	23.8	28.4	17.6	6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.5	53.7	36.2	48.4	62.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: SN54HC08

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	V_{CC} = 2 V	1.9	1.998		V
				V_{CC} = 4.5 V	4.4	4.499		
				V_{CC} = 6 V	5.9	5.999		
			I_{OH} = –4 mA, V_{CC} = 4.5 V	T_A = 25°C	3.98	4.3		
				T_A = –55°C to 125°C	3.7			
			I_{OH} = –5.2 mA, V_{CC} = 6 V	T_A = 25°C	5.48	5.8		
				T_A = –55°C to 125°C	5.2			
V_{OL}	Low-level output voltage	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	V_{CC} = 2 V		0.002	0.1	V
				V_{CC} = 4.5 V		0.001	0.1	
				V_{CC} = 6 V		0.001	0.1	
			I_{OL} = 4 mA, V_{CC} = 4.5 V	T_A = 25°C		0.17	0.26	
				T_A = –55°C to 125°C			0.4	
			I_{OL} = 5.2 mA, V_{CC} = 6 V	T_A = 25°C		0.15	0.26	
				T_A = –55°C to 125°C			0.4	
I_I	Input current	$V_I = V_{CC}$ or 0, V_{CC} = 6 V		T_A = 25°C		±0.1	±100	nA
				T_A = –55°C to 125°C			±1000	
I_{CC}	Quiescent current	$V_I = V_{CC}$ or 0, I_O = 0, V_{CC} = 6 V		T_A = 25°C			2	µA
				T_A = –55°C to 125°C			40	
C_i	Input capacitance	V_{CC} = 2 V to 6 V				3	10	pF

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6.6 Electrical Characteristics: SN74HC08

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_I = V_{IH} or V_{IL}	I_{OH} = –20 µA	V_{CC} = 2 V	1.9	1.998		V
				V_{CC} = 4.5 V	4.4	4.499		
				V_{CC} = 6 V	5.9	5.999		
			I_{OH} = –4 mA, V_{CC} = 4.5 V	T_A = 25°C	3.98	4.3		
				T_A = –55°C to 125°C	3.84			
			I_{OH} = –5.2 mA, V_{CC} = 6 V	T_A = 25°C	5.48	5.8		
				T_A = –55°C to 125°C	5.34			
V_{OL}	Low-level output voltage	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	V_{CC} = 2 V		0.002	0.1	V
				V_{CC} = 4.5 V		0.001	0.1	
				V_{CC} = 6 V		0.001	0.1	
			I_{OL} = 4 mA, V_{CC} = 4.5 V	T_A = 25°C		0.17	0.26	
				T_A = –55°C to 125°C			0.33	
			I_{OL} = 5.2 mA, V_{CC} = 6 V	T_A = 25°C		0.15	0.26	
				T_A = –55°C to 125°C			0.33	
I_I	Input current	V_I = V_{CC} or 0, V_{CC} = 6 V		T_A = 25°C		±0.1	±100	nA
				T_A = –55°C to 125°C			±1000	
I_{CC}	Quiescent current	V_I = V_{CC} or 0, I_O = 0, V_{CC} = 6 V		T_A = 25°C			2	µA
				T_A = –55°C to 125°C			20	
C_i	Input capacitance	V_{CC} = 2 V to 6 V				3	10	pF

6.7 Switching Characteristics: SN54HC08

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay	A	Y	V_{CC} = 2 V	T_A = 25°C		50	100	ns
					T_A = –55°C to 125°C			150	
				V_{CC} = 4.5 V	T_A = 25°C		10	20	
					T_A = –55°C to 125°C			30	
				V_{CC} = 6 V	T_A = 25°C		8	17	
					T_A = –55°C to 125°C			25	
t_t	Transition time		Y	V_{CC} = 2 V	T_A = 25°C		38	75	ns
					T_A = –55°C to 125°C			110	
				V_{CC} = 4.5 V	T_A = 25°C		8	15	
					T_A = –55°C to 125°C			22	
				V_{CC} = 6 V	T_A = 25°C		6	13	
					T_A = –55°C to 125°C			19	

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6.8 Switching Characteristics: SN74HC08

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay	A	Y	V_{CC} = 2 V	T_A = 25°C		50	100	ns
					T_A = –55°C to 125°C			125	
				V_{CC} = 4.5 V	T_A = 25°C		10	20	
					T_A = –55°C to 125°C			25	
				V_{CC} = 6 V	T_A = 25°C		8	17	
					T_A = –55°C to 125°C			24	
t_t	Transition time		Y	V_{CC} = 2 V	T_A = 25°C		38	75	ns
					T_A = –55°C to 125°C			95	
				V_{CC} = 4.5 V	T_A = 25°C		8	15	
					T_A = –55°C to 125°C			19	
				V_{CC} = 6 V	T_A = 25°C		6	13	
					T_A = –55°C to 125°C			16	

6.9 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	No load	20	pF

6.10 Typical Characteristics

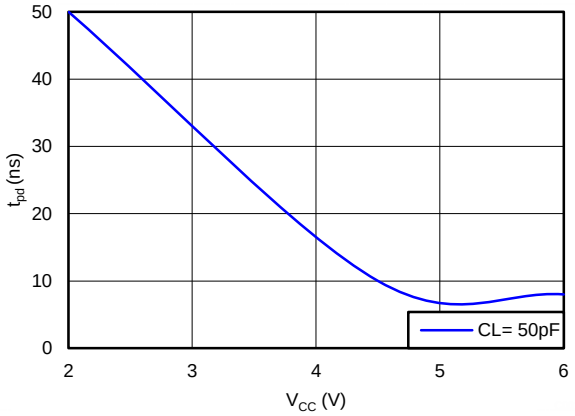
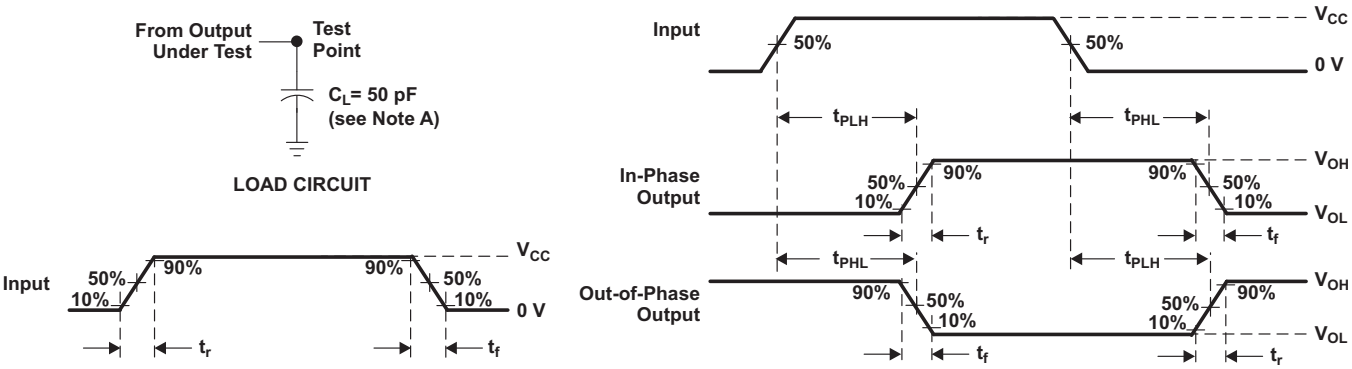


Figure 1. Propagation Delay vs V_{CC}

7 Parameter Measurement Information



A. CL includes probe and test-fixture capacitance.

B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.

C. The outputs are measured one at a time with one input transition per measurement.

D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

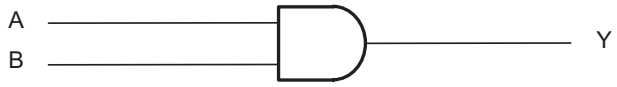
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8 Detailed Description

8.1 Overview

The SNx4HC08 contains quadruple 2-input positive AND gate device and performs the Boolean function Y = A ● B. This device is useful when multiple AND functions are used in the system.

8.2 Functional Block Diagram



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Figure 3. Logic Diagram (Positive Logic)

8.3 Feature Description

The device can operate from 2 V to 6 V, allowing a wide operating voltage.

The device has low power consumption (20-µA maximum I_{CC}).

8.4 Device Functional Modes

Table 1 lists the functional modes for the SN54HC08 and SN74HC08 devices.

Table 1. Function Table (Each Inverter)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

9 Application and Implementation

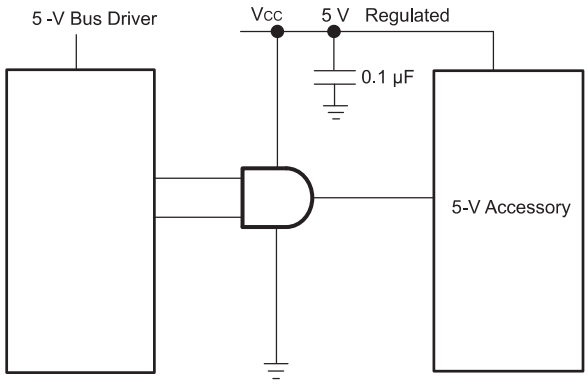
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SNx4HC08 is used to drive CMOS device and used for implementing AND logic. The HC family is low power with the SNx4HC08 having 20-µA maximum supply current. The supply for SN74HC08 is wide, accepting 2-V to 6-V V_{CC}. This device can be used for a multitude of bus-interface type applications where output ringing is a concern.

9.2 Typical Application



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Figure 4. Typical Application Diagram

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so consider routing and load conditions to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended input conditions
   - Rise time and fall time specs: See (Δt/ΔV) in *Recommended Operating Conditions*.
   - Specified high and low levels: See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
2. Absolute Maximum Output Conditions
   - Load currents must not exceed 25 mA per output and 50 mA total for the part
   - Outputs must not be pulled above V_{CC}

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Typical Application (continued)

9.2.3 Application Curve

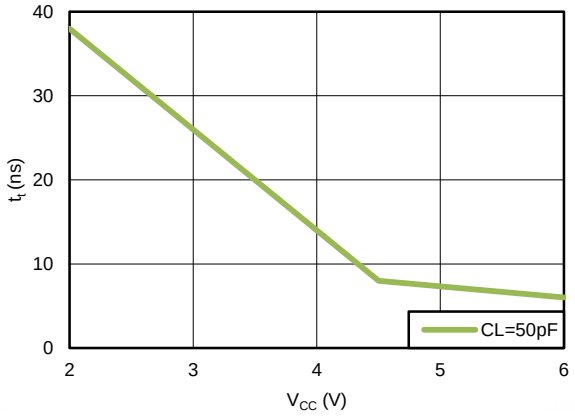


Figure 5. Transition Time vs V_{CC}

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*.

Each VCC pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended and if there are multiple VCC pins then 0.01-µF or 0.022-µF capacitor is recommended for each power pin. Multiple bypass capacitors may be used in parallel to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or VCC, whichever makes more sense or is more convenient.

11.2 Layout Example

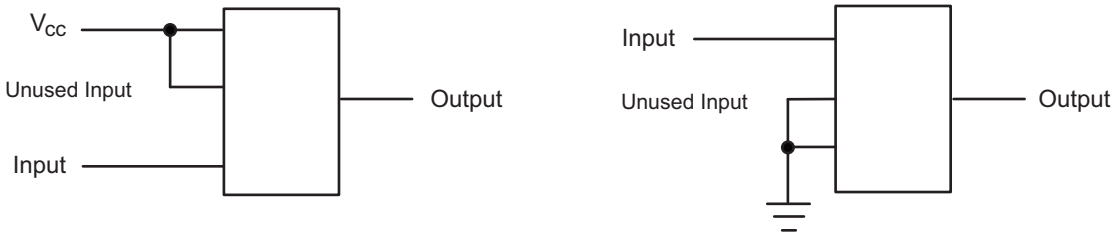


Figure 6. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC08	Click here	Click here	Click here	Click here	Click here
SN74HC08	Click here	Click here	Click here	Click here	Click here

12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8404701VCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8404701VC A SNV54HC08J	Samples
5962-8404701VDA	ACTIVE	CFP	W	14	25	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8404701VD A SNV54HC08W	Samples
84047012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84047012A SNJ54HC 08FK	Samples
8404701CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8404701CA SNJ54HC08J	Samples
8404701DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8404701DA SNJ54HC08W	Samples
JM38510/65203B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 65203B2A	Samples
JM38510/65203BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65203BCA	Samples
JM38510/65203BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65203BDA	Samples
M38510/65203B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 65203B2A	Samples
M38510/65203BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65203BCA	Samples
M38510/65203BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65203BDA	Samples
SN54HC08J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54HC08J	Samples
SN74HC08D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC08	Samples
SN74HC08DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC08	Samples
SN74HC08DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC08	Samples
SN74HC08DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC08	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC08DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	HC08	Samples
SN74HC08DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC08	Samples
SN74HC08DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC08	Samples
SN74HC08DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC08	Samples
SN74HC08DTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC08	Samples
SN74HC08N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC08N	Samples
SN74HC08NE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC08N	Samples
SN74HC08PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC08	Samples
SN74HC08PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC08	Samples
SN74HC08PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	HC08	Samples
SN74HC08PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC08	Samples
SN74HC08PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC08	Samples
SN74HC08PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC08	Samples
SNJ54HC08FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84047012A SNJ54HC 08FK	Samples
SNJ54HC08J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8404701CA SNJ54HC08J	Samples
SNJ54HC08W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	8404701DA SNJ54HC08W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC08, SN54HC08-SP, SN74HC08 :

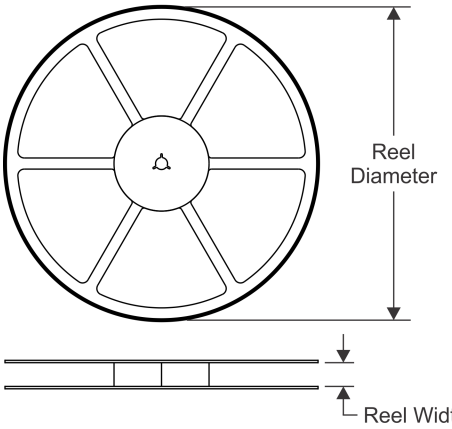
- Catalog: SN74HC08, SN54HC08
- Automotive: SN74HC08-Q1, SN74HC08-Q1
- Military: SN54HC08
- Space: SN54HC08-SP

NOTE: Qualified Version Definitions:

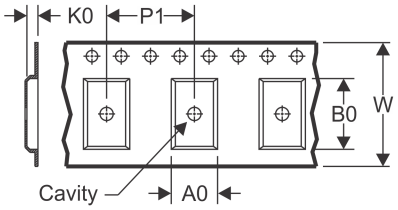
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

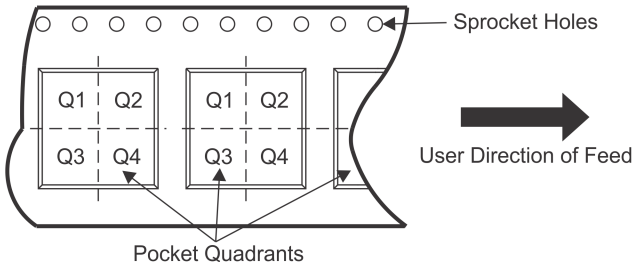


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

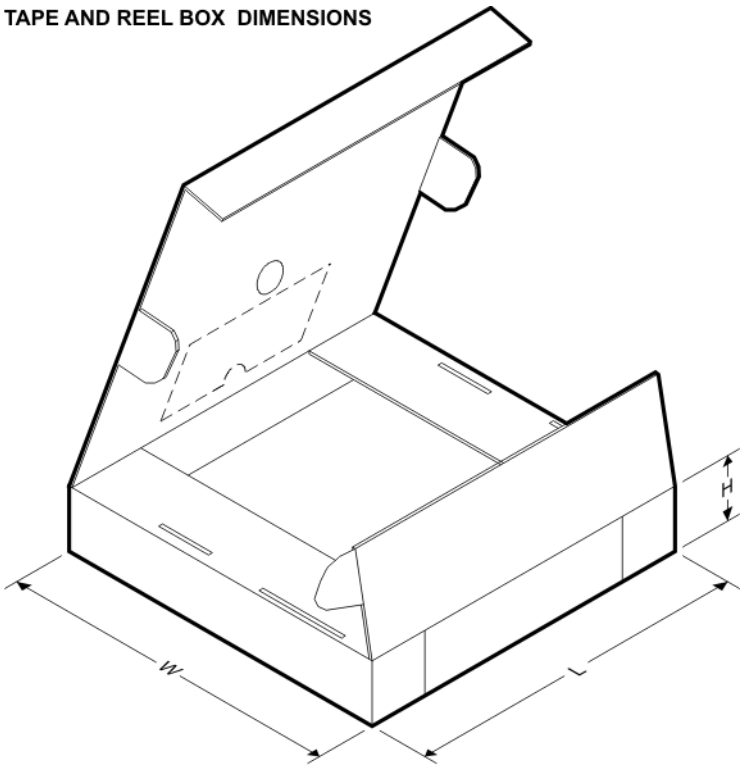
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC08DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC08DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
SN74HC08DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC08DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC08DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC08DT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC08PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC08PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC08PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC08PWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

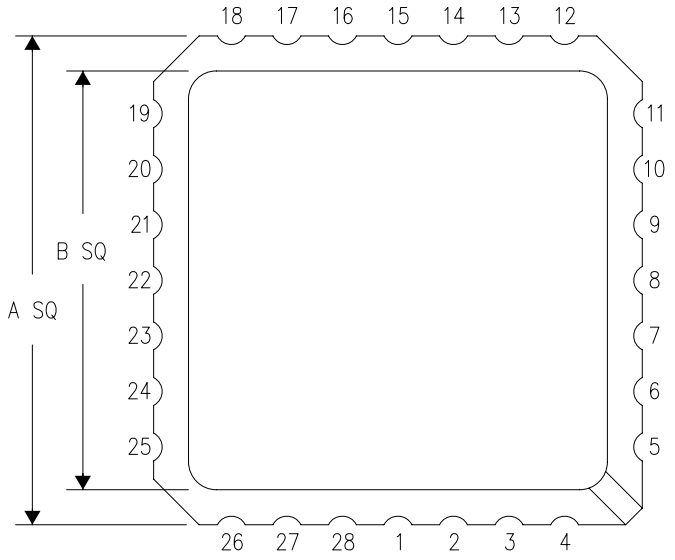


*All dimensions are nominal

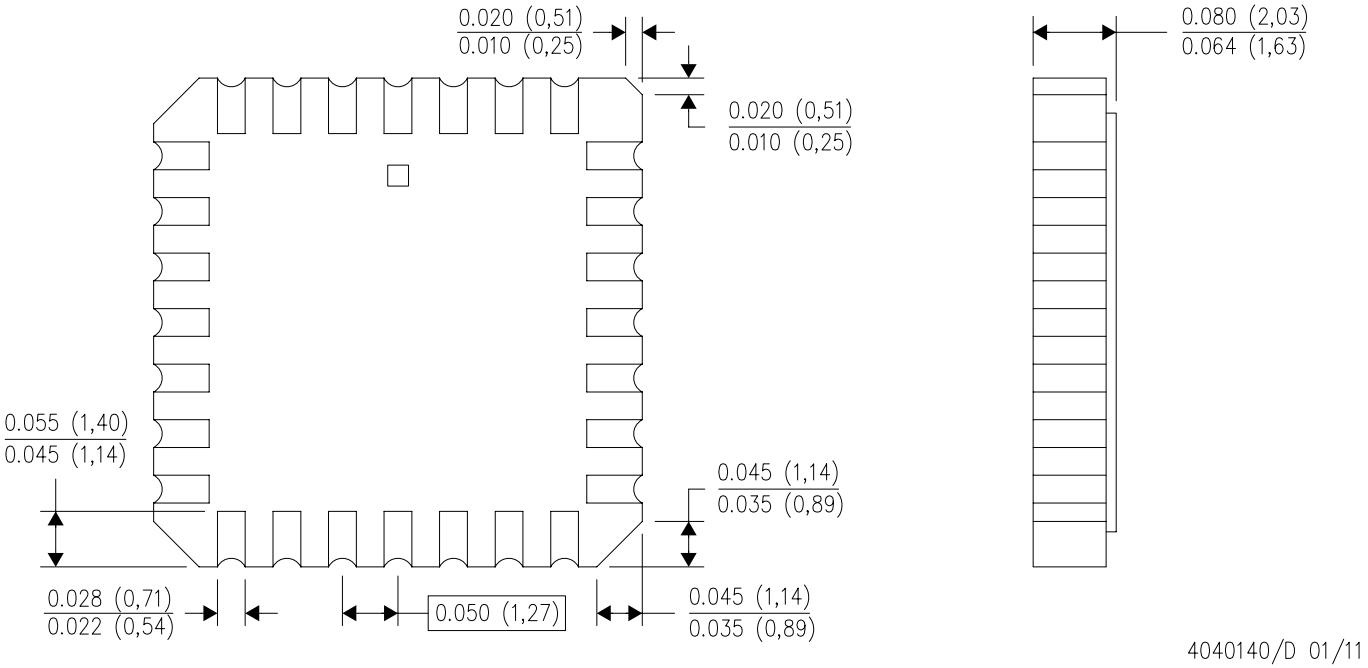
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC08DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC08DR	SOIC	D	14	2500	364.0	364.0	27.0
SN74HC08DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC08DRG4	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC08DRG4	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC08DT	SOIC	D	14	250	210.0	185.0	35.0
SN74HC08PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HC08PWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74HC08PWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HC08PWT	TSSOP	PW	14	250	367.0	367.0	35.0

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



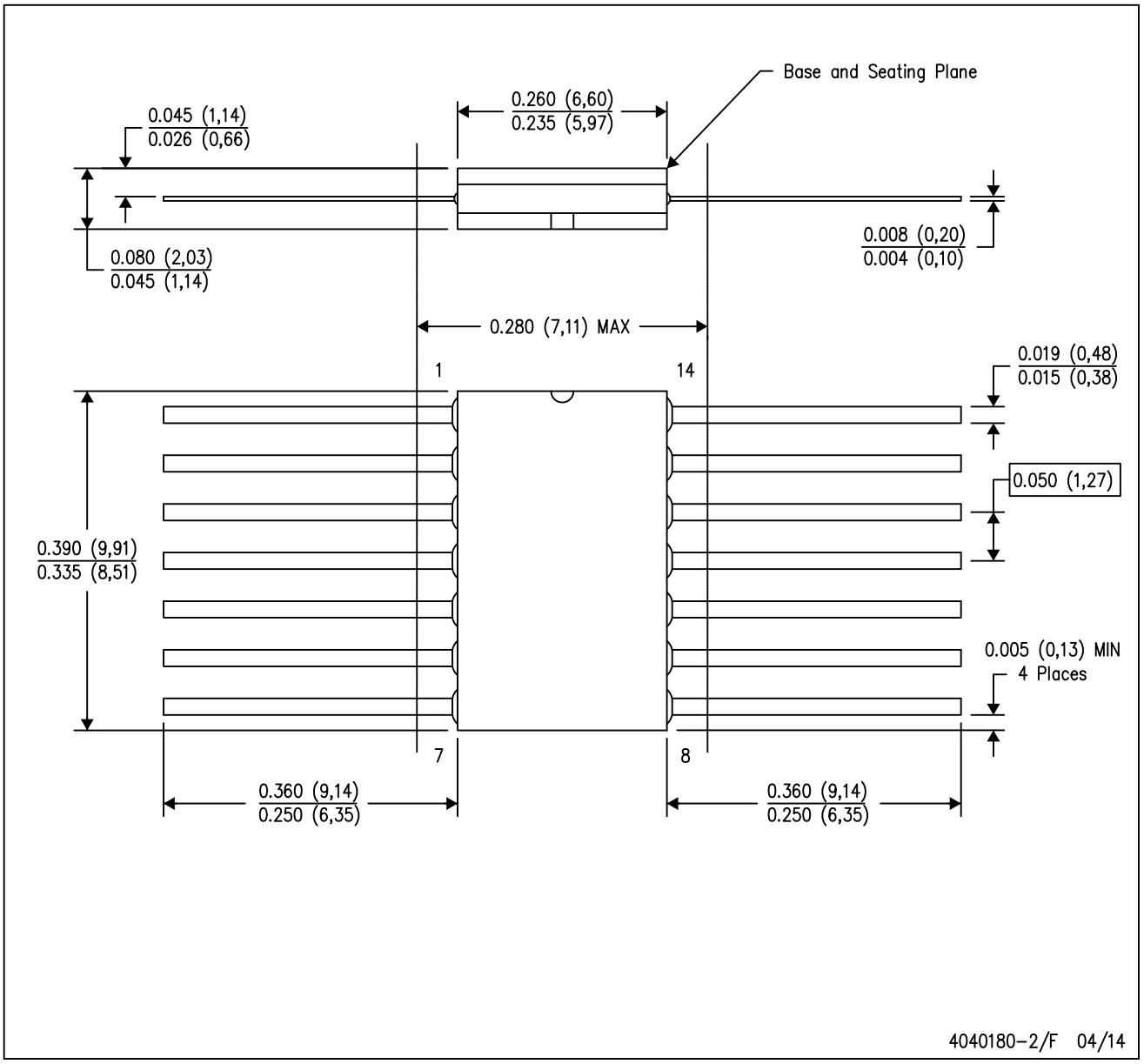
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

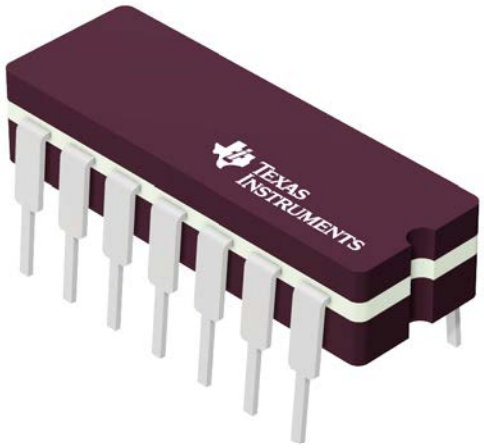


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

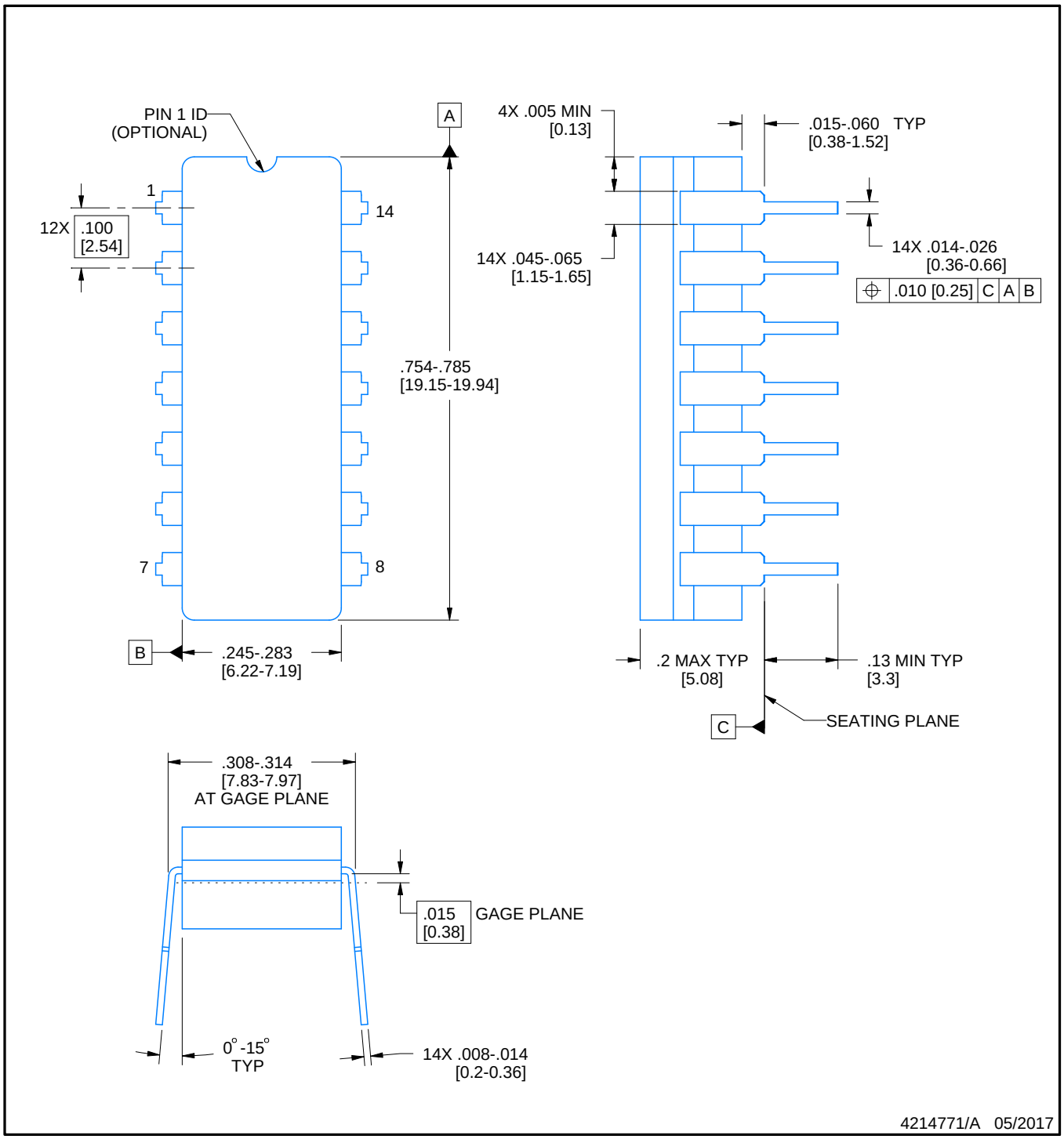


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

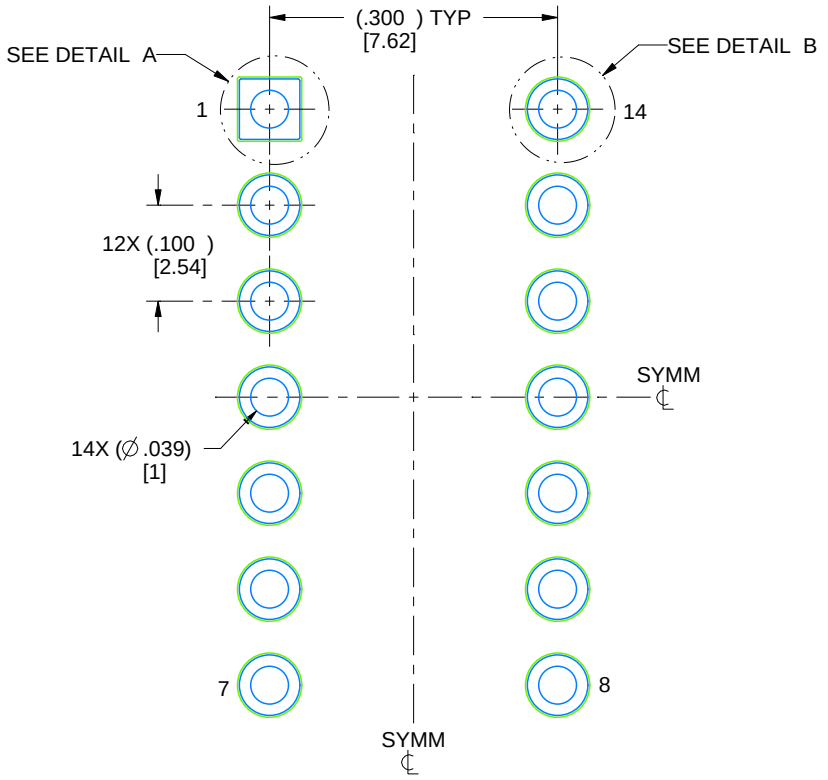
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

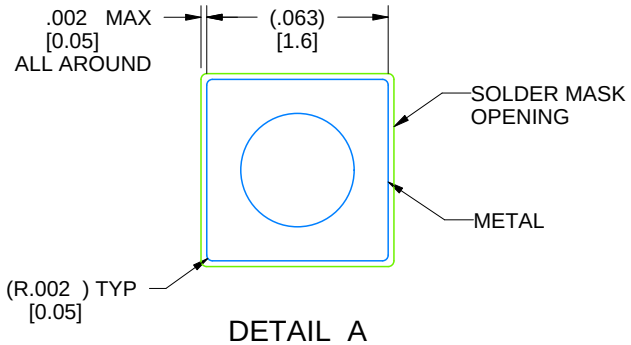
J0014A

CDIP - 5.08 mm max height

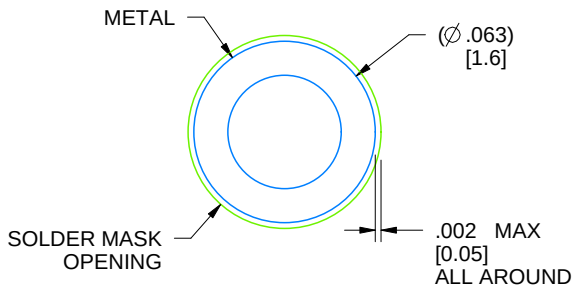
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



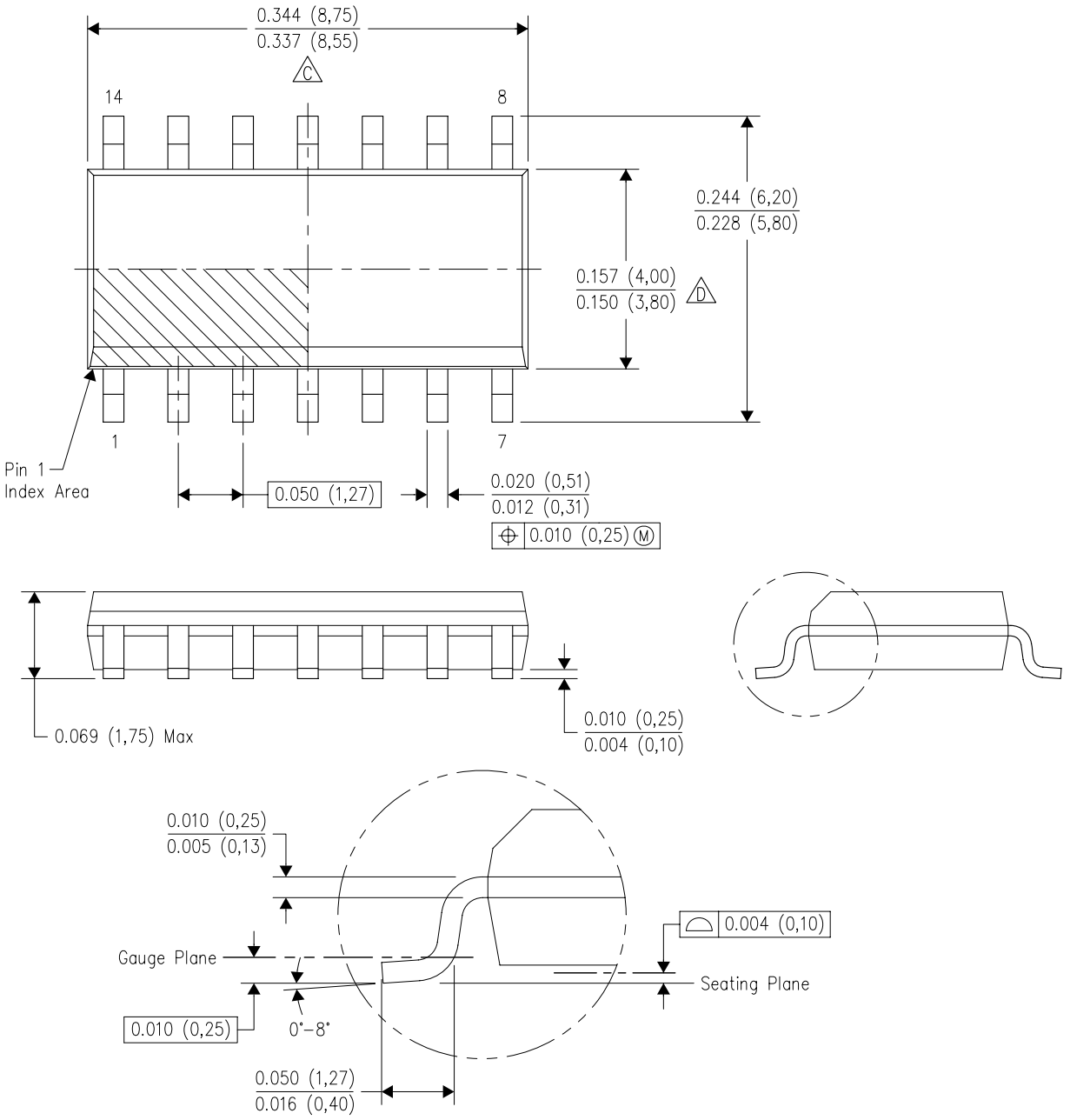
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

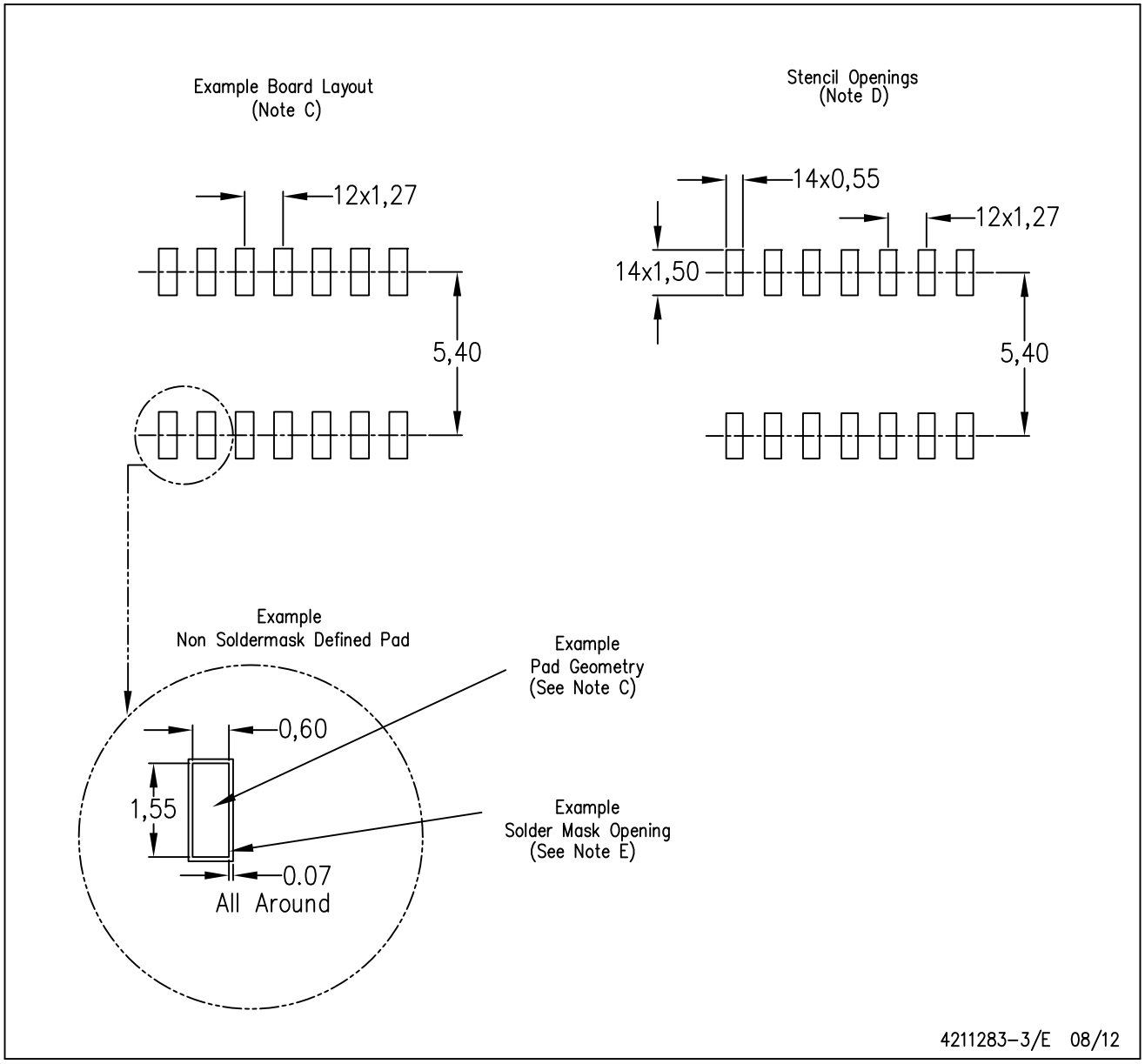
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

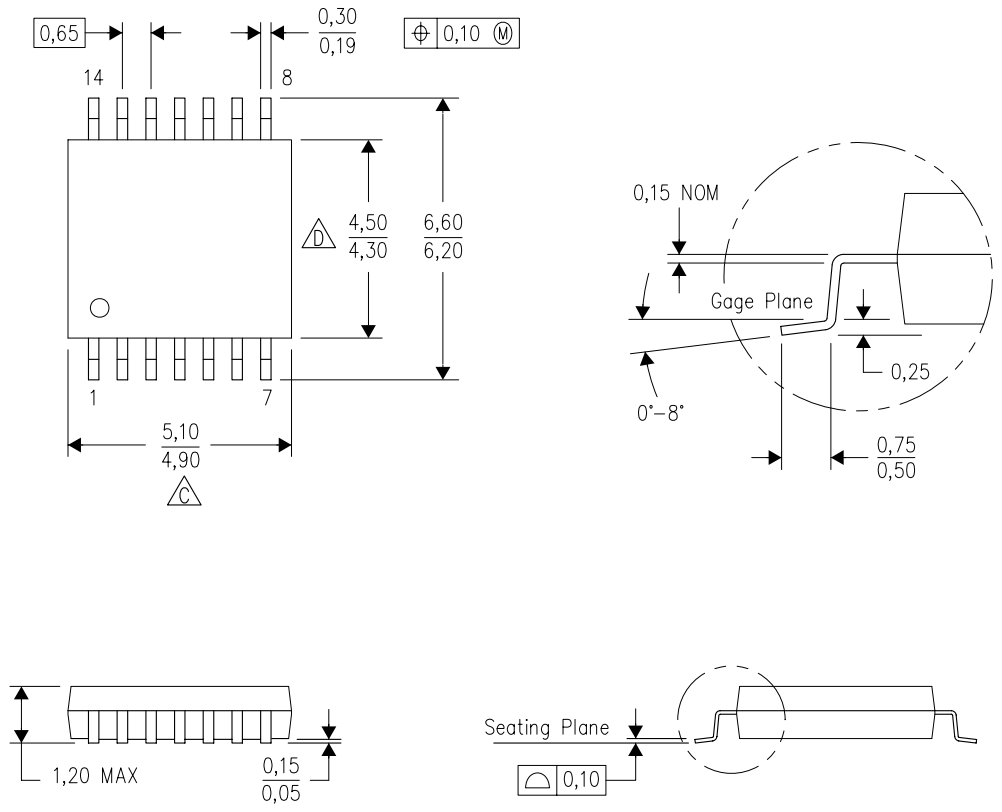
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

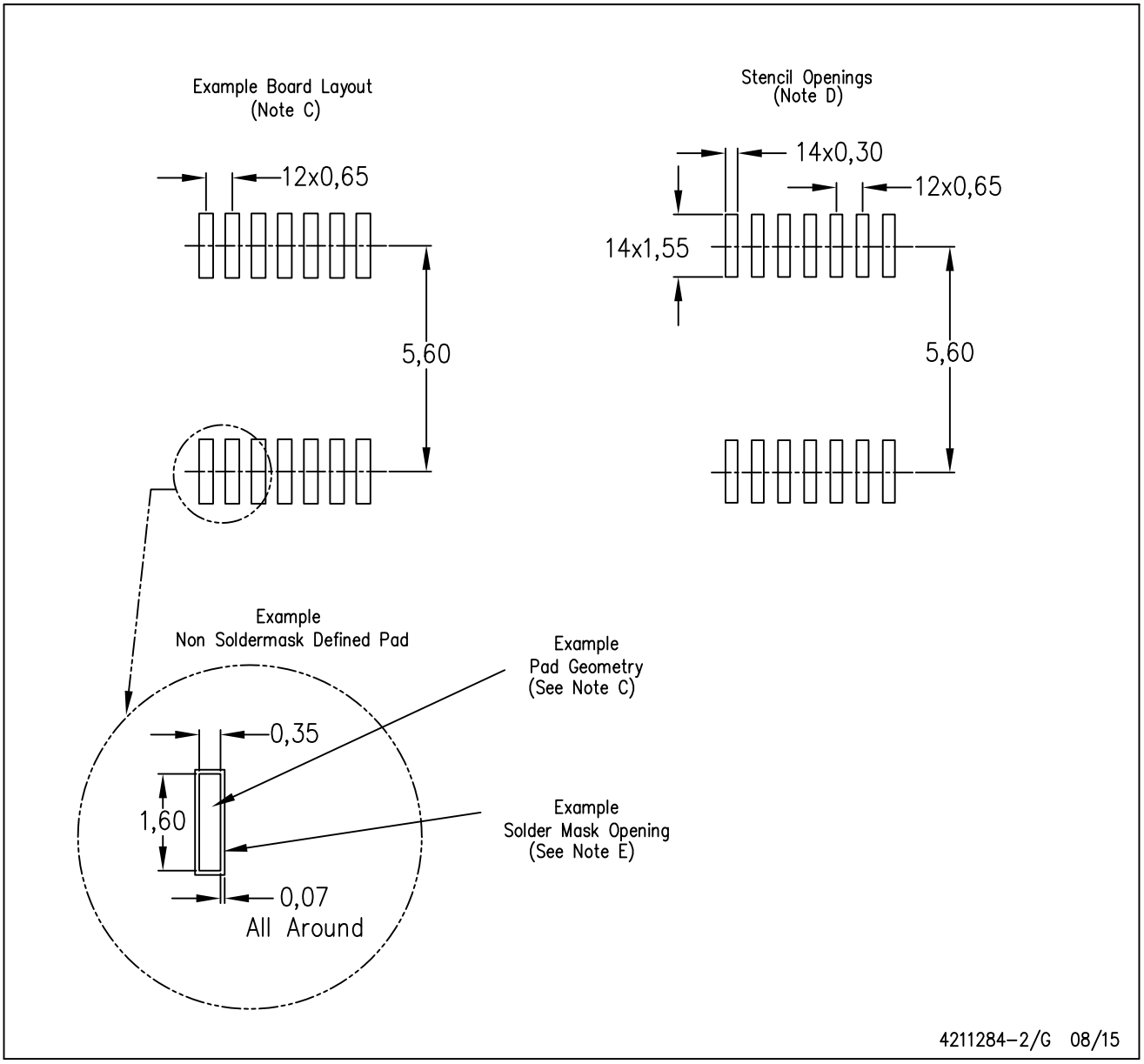
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

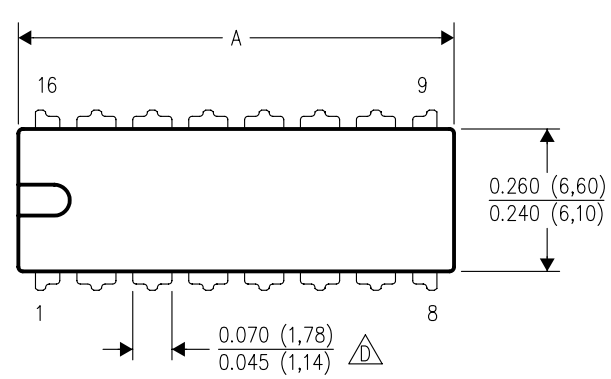


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

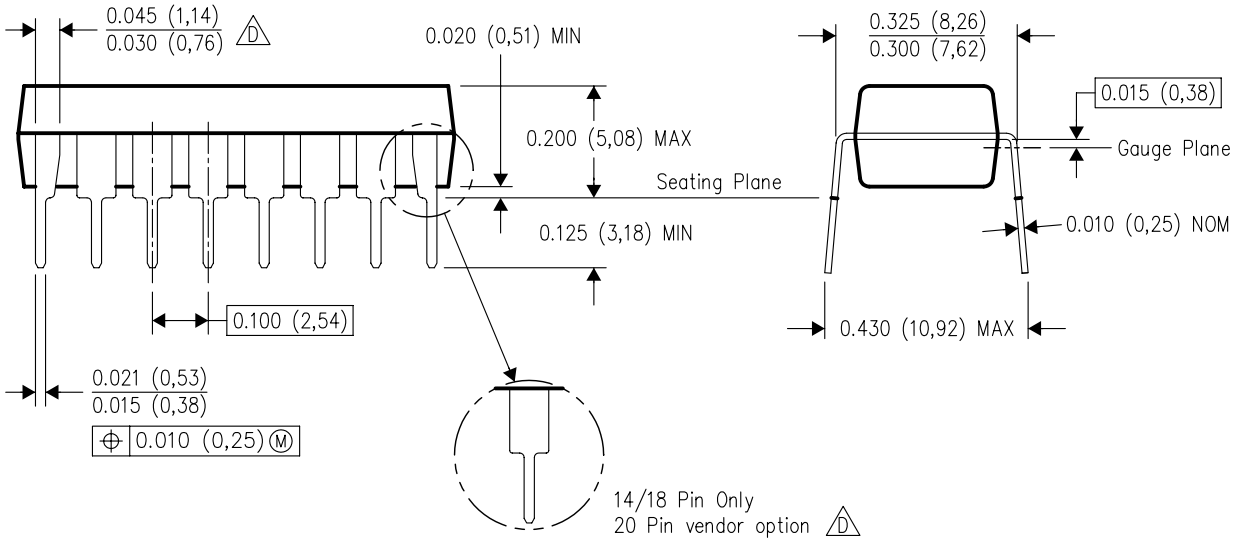
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



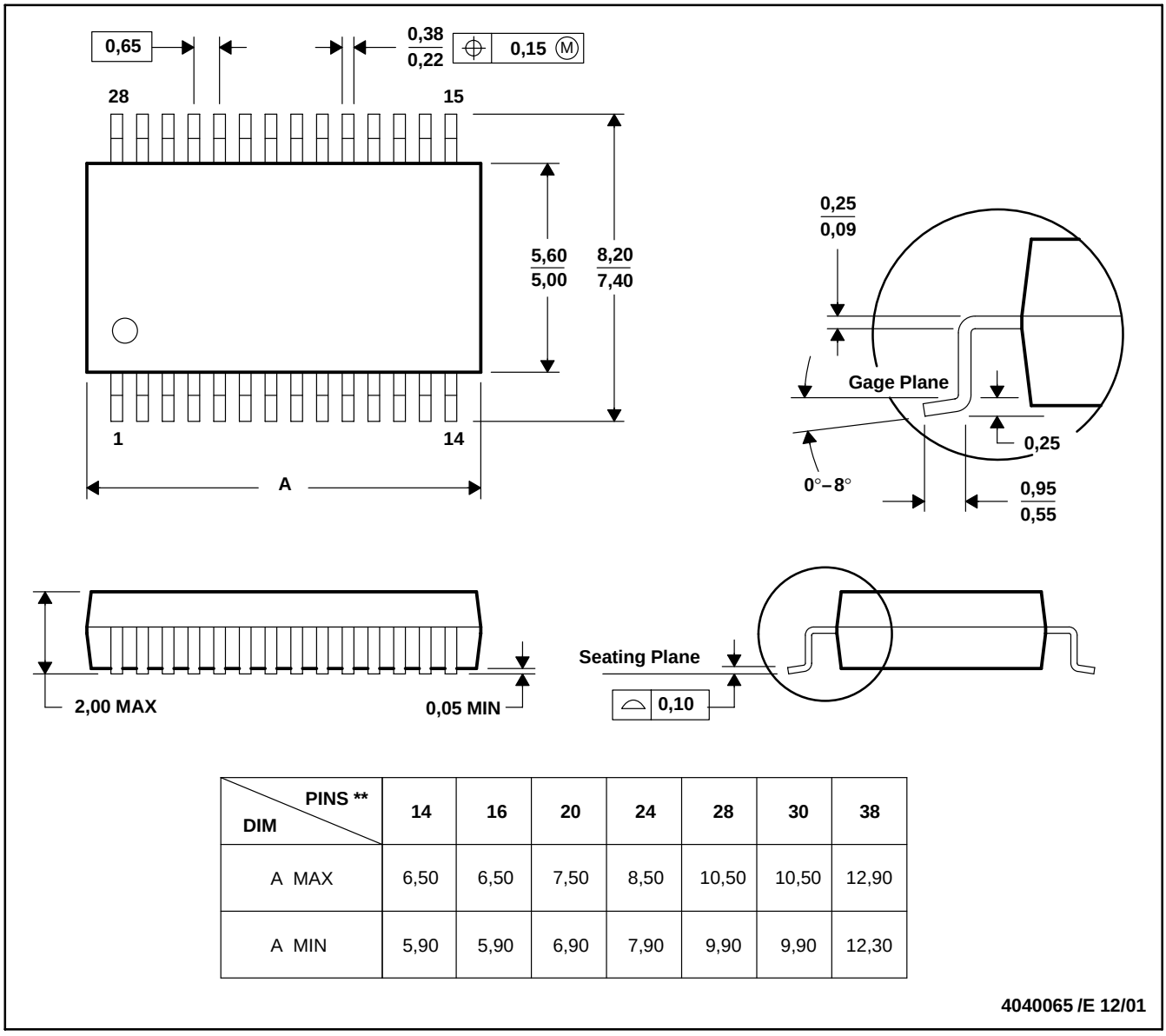
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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